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EDUCATION SERVICES
COURSE LISTING

EDUCATION SERVICES
Xilinx Global Services

Xilinx Education Services courses dramatically reduce your time to knowledge, which improves your design efficiency and reduces your overall development costs.

FPGA DESIGN

Fundamentals of FPGA Design
Level: Fundamental **Duration:** 1 day **Credits (Israel):** 3 **Cost:** US $300

Understand Xilinx FPGA architecture and learn to implement a complete design in one day. This course provides you with an introduction to designing with Xilinx FPGAs using Xilinx ISE. Features covered in this course include the Architecture Wizard, assistance in assigning pins, and creating area constraints (PACE). Other topics include design planning, implementation options, and global timing constraints. Reduce your learning curve through several practical labs.

Designing for Performance
Level: Intermediate **Duration:** 2 days Credits **(Israel):** 6 **Cost:** US $600

Learn design techniques to help improve your design's performance. This course builds on the principles covered in our Fundamentals of FPGA Design course with an emphasis on achieving timing closure. Topics include FPGA design techniques, HDL coding techniques, the CORE Generator™ system, power estimation, timing analysis, advanced timing constraints, and advanced implementation options. This course is also offered periodically live online.

Advanced FPGA Implementation
Level: Advanced **Duration:** 2 days **Credits (Israel):** 6 **Cost:** US $600

Push the limits of your design by learning design techniques that will increase your overall proficiency. This course builds on the principles covered in our Fundamentals of FPGA Design and Designing for Performance courses. Some of the concepts that you will learn include incremental and modular design techniques, creating floorplans, using scripting, implementing relationally placed macros, editing and simplifying constraints files, using FPGA Editor for advanced implementation editing, and using clock resources effectively.

Designing with the Virtex™-4 Family

Level: Intermediate **Duration:** 2 days **Credits (Israel):** 6 **Cost:** US $600

Interested in learning how to effectively utilize Virtex-4 architectural resources? Targeted towards experienced Xilinx users who have already completed Fundamentals of FPGA Design and Designing for Performance, this course focuses on understanding as well as designing into several of the new and enhanced resources found in our newest device. Features covered include V-4 overview, DCM and PMCD, global and regional clocking techniques, memory and FIFO, and source synchronous resources. A combination of modules and labs allow for practical hands-on application of the principles taught.

DSP DESIGN

DSP Design Flow

Level: Intermediate **Duration:** 3 days **Credits (Israel):** 9 **Cost: US** $900

XtremeDSP™ is the World's Fastest Programmable DSP Solution. This course covers the Xilinx design flow for implementing DSP functions.

The main focus of this course is on the System Generator for DSP. The class also includes information on HDL design flow, the CORE Generator system, design implementation tools, software simulation, and hardware-in-the-loop verification using a demo board. You will gain extensive experience with system-level design while also becoming familiar with Xilinx FPGA capabilities and learning how to implement a design from algorithm concept to hardware verification.

DSP Implementation Techniques

Level: Advanced **Duration:** 3 days **Credits (Israel):** 9 **Cost:** US $900

This course bridges the gap between the DSP algorithm/system designer and the hardware engineer. While describing how algorithms can be efficiently implemented, the course techniques also demonstrate which decisions, at the system level, have the greatest impact on the implementation process, resource costs, and performance.

HIGH-SPEED DESIGN

Designing with Multi-Gigabit Serial I/O

Level: Intermediate **Duration:** 2 days **Credits (Israel):** 6 **Cost:** US $600

Learn how to employ RocketIO™ in your Virtex-II Pro™ design. Understand and utilize the features of the RocketIO transceiver blocks, such as CRC, 8b/10b encoding, channel bonding, clock correction, and comma detection. Additional highlighted topics include debugging techniques, use of the Architecture Wizard, synthesis and implementation considerations, and standards compliance. This comprehensive course equally balances lecture modules with practical hands-on lab work.

Signal Integrity for High-Speed Memory and Processor I/O –

Level: Intermediate **Duration:** 2 days **Credits (Israel):** 6 **Cost: US** $600

Learn how signal integrity techniques are applicable to high-speed interfaces between Xilinx FPGAs and semiconductor memories.

This course teaches you about high-speed bus and clock design, including transmission line termination, loading, and jitter. You will work with IBIS models and complete simulations using CAD packages. Other topics include managing PCB effects and on-chip termination. This course balances lecture modules and practical hands-on labs.

EMBEDDED SYSTEMS DESIGN

Embedded Systems Development

Level: Intermediate **Duration:** 2 days **Credits (Israel):** 6 **days Cost:** US $600

Embedded Systems Development brings experienced FPGA designers up to speed on the capabilities and characteristics of the Xilinx MicroBlaze™ 32-bit soft processor core, the hard embedded IBM PowerPC™ core in the Virtex-II Pro™ FPGA, and the Embedded Development Kit (EDK) design environment. Developing embedded systems using the hard or soft processor cores and a set of soft peripherals is also included in the lectures and labs. Plentiful personal experience with the development, debugging, and simulation of the embedded system is provided in the "hands on" labs.

LANGUAGES

Introduction to Verilog

Level: Fundamental **Duration:** 3 days **Credits (Israel):** 9 days **Cost:** US $900

This comprehensive course is an effective introduction to the Verilog language. Course emphasis includes targeting Xilinx FPGA devices as well as simulation techniques. The information gained here can be applied to any digital design by using a top-down synthesis approach. This course couples insightful lecture modules with practical lab exercises to reinforce key concepts.

Introduction to VHDL

Level: Fundamental **Duration:** 3 days **Credits (Israel):** 9 days **Cost:** US $900

This comprehensive course is an effective introduction to the VHDL language. Course emphasis includes targeting Xilinx FPGA devices as well as simulation techniques. The information gained here can be applied to any digital design by using a top-down synthesis design approach. The course couples insightful lecture modules with practical lab exercises to reinforce key concepts.

Advanced VHDL

Level: Advanced **Duration:** 2 days **Credits (Israel):** 6 **days Cost:** US $600

Increase your VHDL proficiency by learning advanced techniques to help you write more robust and reusable code. This comprehensive course is targeted towards designers who already have some experience with VHDL. The course highlights modeling, test benches, RTL/synthesizable design, and techniques aimed at creating parameterizable and reusable designs. The majority of class time is spent in challenging hands-on labs, as compared to lecture modules.

PCI DESIGN

PCI Core Basics

Level: Fundamental **Duration:** 1 day **Credits (Israel):** 3 **days Cost:** US $300

This PCI training course gives you an introduction to basic PCI concepts and architecture. The course emphasizes and illustrates how PCI transactions take place. It also gives an overview of Xilinx PCI solutions and includes a lab that illustrates the general design flow from core to verification. This course is also offered periodically live online.

Designing a LogiCORE PCI System

Level: Intermediate **Duration:** 2 days **Credits (Israel):** 6 **days Cost:** US $600

Learn the tips and tricks of PCI design in this two-day course, which provides an introduction to basic PCI concepts and architecture as well as intensive training on designing with the PCI core for Xilinx. This course emphasizes and illustrates how PCI transactions take place, and gives you an overview of Xilinx PCI solutions. You will learn the basics of Xilinx PCI cores including PCI 64/66 and PCI 32. You will also learn design concepts and basic verification strategies for creating a PCI system design. The labs cover the basic transaction analysis using the ModelSim™ simulator and the general design flow, from core to verification using ISE 6.2.

Designing for PCI-X

Level: Intermediate **Duration:** 2 days **Credits (Israel):** 6 **Cost: US** $600

This course focuses on the PCI-X 2.0 specification and provides a detailed investigation into the operation of the PCI-X LogiCORE. The emphasis is on how PCI-X transactions take place, including a brief review of PCI protocol fundamentals. Explaining the principles and concepts introduced by the PCI-X Addendum, this course also provides an in-depth understanding of the PCI-X LogiCORE™ and how a digital designer may interface this to a typical user application to create a flexible PCI-X solution. This course is also offered periodically live online.